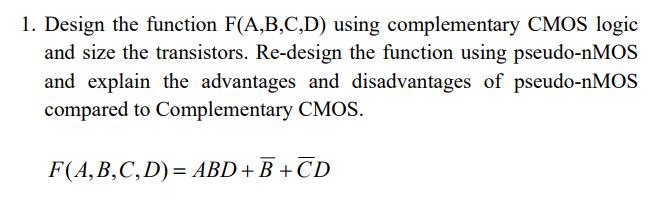
ETICD-01 Introduction to IC Design

ETICD Hand-in assignment #1

Group 3

October 14, 2017



First the truth table and Karnaugh map have been worked out for function

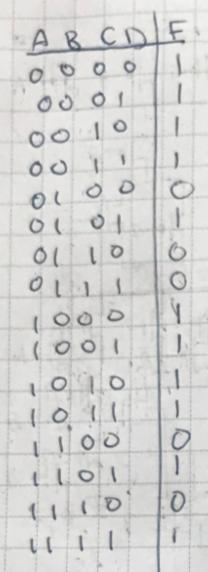


Figure 1 Truth table for F(A,B,C,D)

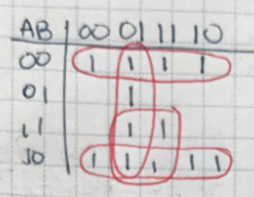


Figure 2 Karnaugh map for F(A,B,C,D)

Now the complementary CMOS design

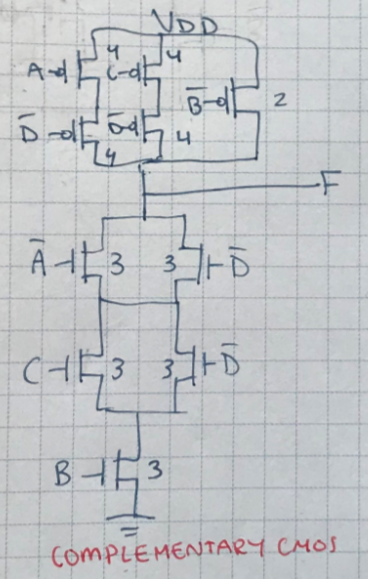


Figure 3 Complementary CMOS design of F(A,B,C,D)

The Complementary CMOS design is now reduced to a pseudo-nMOS by replacing the pMOS section with a single pMOS tied to gound.

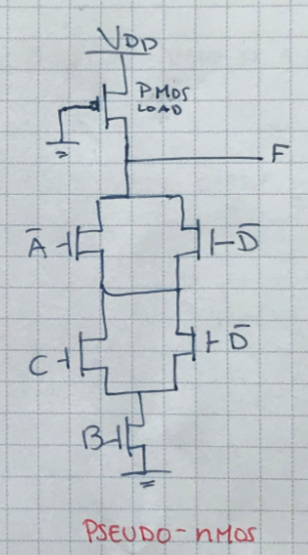


Figure 4 pseudo-nMOS design of F(A,B,C,D)

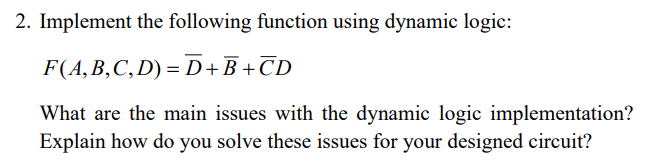
By replacing the complimentary CMOS with a pseudo-nMOS design, both some advantages and disadvantages follows:

Advantages of pseudo-nMOS

* Ability to control the speed of the system by sizing the pMOS
* Fewer transistors = smaller area
* Smaller load because of smaller parasitic capacitance
* Reduced noise margins

Disadvantages of pseudo-nMOS

* Static power dissipation



Implementation of function is as follows

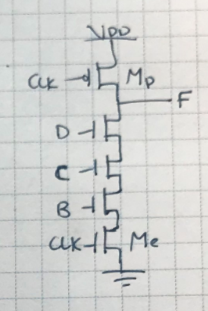


Figure 5 Implementation of F(A,B,C,D)

By implementing the function this way, the circuit will have a charge leakage. When the nMOS transistor is off there will be a leakage current running from the source to the drain.  
Furthermore the circuit will have an issue with power dissipation, which is usually higher than static CMOS.

To solve these issues a keeper circuit is added on the output F. This helps keeping the output high when the circuit is in evaluation. Sizing of the transistors is important when using a keeper circuit so the nMOS transistor can pull the circuit down.

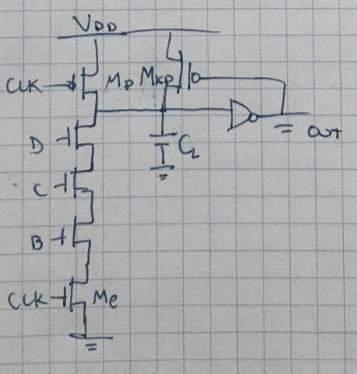
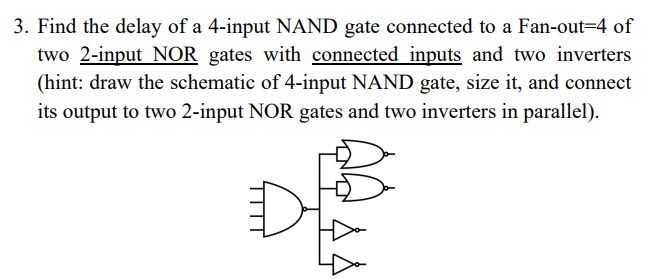


Figure 6 Implementation of function F(A,B,C,D) with a keeper circuit added on the output



By using the formulas for logical effect , electrical effect , delay , and absolute delay with a table lookup for parasitic delay , the delay of the of the 4-input NAND gate can be determined.

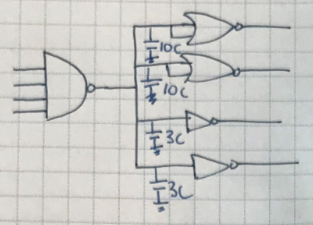
Before the delay is determined the schematic is sized:  


Figure 7 Sized schematic of the circuit

Now the delay of the 4-input NAND gate is determined.  
Logical effort:

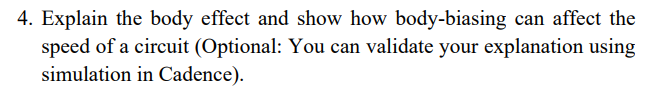
Electrical effort:

Parasitic delay:  
The parasitic delay for a 4-input NAND gate is

Delay:

Absolute delay:

The delay of the 4-input NAND gate is therefore .



The Body effect of a transistor, is created when a voltage is appplied between the source and body, making a fourth terminal, this effect is mainly based on the size of the transistor. This fourth terminal increases the charge reguired to shift the channel, thereby increasing the threshold voltage(Vth).

An additional effect that increasing Vth has is determining a transistors pass characteristics. nMOS transistors pass 1’s poorly, making the voltage level off the 1 Vdd- Vth this fall in voltage can potentially violate the noise margins off the transistor especially in circuits with low voltage. For pMOS transistors it has the opposite effect making them pass 0’s poorly.

*How can body biasing affect the speed of a circuit?*

To answer this we take a standard pseudo-nMOS circuit.

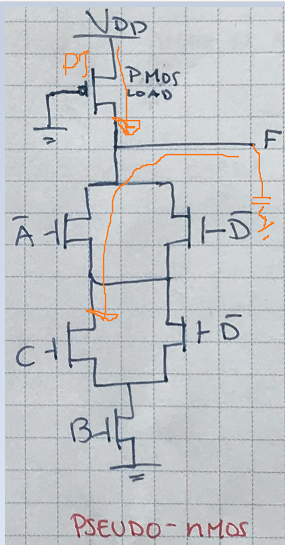


Figure 8 Standard Pseudo-nMOS

As we can see in the circuit the nMOS area is open, and the circuit is trying to discharge the load. However the PMOS transistor P1 is always on and therefore always trying to charge the load. Whether we are discharging or charging is therefore determined by which current is stronger. Therefore the circuit must be made so that the nMOS’s have a stronger current, to discharge, but even if this is the case, the size and therefore amount of current P1 can draw, will affect the speed that the nMOS transistors can discharge the load. So often this pMOS must be smaller so that the performance of the circuit is maintained.